sequentially etching the top semiconductor layer, the oxide layer, the bottom semiconductor layer and the bottom conductor layer.

125. (New) A process for fabricating a pillar in a 3-D semiconductor memory device, wherein the pillar includes a steering element and a state change element vertically arranged between orthogonally disposed conductors leads, the process comprising the steps of:

forming a semiconductor layer; and

oxidizing at least a portion of the semiconductor layer in a plasma to form an oxide antifuse layer overlying the semiconductor layer.

REMARKS

Claims 95-125 are pending in the application. Claims 95, 107, and 111 have been amended, claims 116-125 are newly added, and claims 101-106 have been withdrawn pursuant to a restriction requirement. No new matter has been added by the amendment.

Rejection Under 35 U.S.C. §112, second paragraph

Claim 111 has been rejected for failure to provide antecedent basis for the term "steering element." The rejection is believed overcome in view of the amendment of claim 111 replacing the term "steering element" with "conductor layer."

Rejection Under 35 U.S.C. §102(e)

Claims 95 and 97-100 have been rejected over McCollum et al. This rejection is believed overcome in view of the amendment of claim 95 together with the following remarks.

The applicants respectfully assert that to anticipate their claims McCollum et al. must disclose each and every step the applicants' process exactly as claimed. In contrast to the process disclosed by McCollum et al., the applicants' claims are directed to a process for fabricating components in a 3-D semiconductor device. Claim 1, as amended, recites a process that includes fabricating multiple memory layers in a vertically fabricated memory cell. Such a process is not suggested or disclosed by McCollum et al.

In contrast to the process claimed by applicants, McCollum et al. disclose a process for fabricating a 2-D semiconductor device. Such a process does not involve the fabrication details of a multi-layered structural device. For example, in the applicant's process several memory layers must be sequentially fabricated, whereas the process described by McCollum et al. involves only a single functional memory layer. The process dynamics substantially differ where underlying layers contain many components assembled from semiconductor and metal elements, many of which contain dopants and mobile species that can cause the memory device to fail if they diffuse through subjection to excessive heat while fabricating the overlying memory layers. Since McCollum et al. do not suggest or disclose a process for fabricating multiple memory layers, McCollum et al. cannot anticipate claim 95.

Claims 96-100 recite additional process limitations and are believed allowable in view of the amendment and remarks pertaining to claim 95 from which they depend.

Rejection Under 35 U.S.C. §103(a)

Claims 107, 109, and 112-115 have been rejected over McCollum et al. in view of Hart et al. This rejection is believed overcome in view of the amendment of claim 107 together with the following remarks.

Claim 107, as amended, recites a process in which a 3-D semiconductor memory device is fabricated in which a pillar is formed by a

self-aligned etching process. The pillar by first forming a first and second semiconductor layers having and intermediate plasma oxide layer, then sequentially etching these layers to form a line. A second conductor layer is formed to overlie the line and the layers are again etched to form the pillar. Such a process is not suggested or disclosed by the combination of cited references.

As set forth above, McCollum et al. do not disclose fabrication of a multi-layer memory device. Accordingly, McCollum et al. do not teach the formation of a pillar since this structure is an element of a 3-D memory device. The addition of Hart et al. does not overcome the deficiency of McCollum et al. Neither Hart et al. nor McCollum et al. suggest or disclosure the fabrication of a pillar in a 3-D memory device.

Claims 109 and 112-115 recite additional process limitations and are believed allowable in view of the amendment and remarks pertaining to claim 107 from which they depend.

Claim 97 and 108 have been rejected over McCollum et al. in view of Miyasaka. This rejection is believed overcome in view of the amendment and remarks pertaining to claim 95 from which claim 97 depends, and claim 107 from which claim 108 depends. The applicants assert that Miyaska does not overcome the deficiency of McCollum et al. at least because Miyaska does not suggest or disclose a process for fabricating a 3-D memory device containing multiple memory layers or pillars.

The additionally cited references have been carefully examined and found not to be relevant to the applicants' claimed invention.

New Claims

Claims 116-125 are newly added in order that applicants may more fully claim the memory fabrication process of their invention. The applicants assert that these claims fully distinguish over the prior art of record.

Claim 116 recites a process for fabricating a single element antifuse in a 3-D memory device. The antifuse is formed by plasma oxidizing an active electrode layer, then forming a second active electrode layer contacting the oxide antifuse. This process distinguishes over the cited prior art at least because the cited references teach a process that forms anitifuses using multiple components that include inactive semiconductor layers.

New claims 117-118 depend from claim 116 and recite that the active layers are anodes and cathodes of the memory device.

Claim 119 depends from claim 116 and adds the formation of orthogonally disposed conductors to the claimed process. Orthogonally disposed conductors provide electrical interconnection in the applicants' 3-D memory device and are not disclosed in the 2-D devices of the cited prior art.

Claim 120 recites a process for forming first and second overlying stacks where each stack includes a state change element. Such a structure is not suggested or disclosed in the cited prior art.

Claim 121 recites the formation of orthogonally disposed conductor layer above and below each memory stack. Again, such a fabrication process is not suggested in the cited references.

Claim 122 recites a detailed process for the fabrication of a 3-D memory device that includes the formation of a pillar. The device is formed by depositing a first semiconductor layer, an oxide layer, and a second semiconductor layer, and etching these layers twice to form a pillar. A sidewall region is created on the pillar using a plasma oxidation process. These steps are not suggested or disclosed by the cited references. The cited references do not suggest or disclose, *inter alia*, neither the formation of a pillar nor the formation of edge regions using plasma oxidation.

Claim 123 recites a process for fabricating a 3-D semiconductor memory device that includes a second stack overlying a first stack. The first and second stacks form a pillar in the 3-D memory device. A plasma oxidation process is used to from an edge region on the pillar. None of the

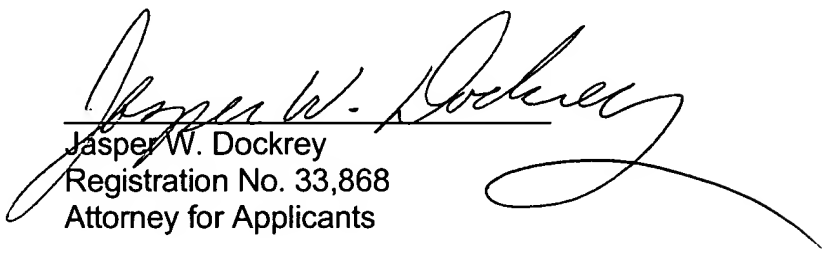
cited references suggest or disclose neither the fabrication of a pillar nor the formation of edge regions on the pillar using a plasma oxidation process.

Claim 124 depends from claim 123 and recites a detailed process for fabricating the first stack.

Claim 125 recites a process for fabricating a 3-D semiconductor memory device that includes a pillar comprised of a steering element and a state change element vertically arranged between orthogonally disposed conductor leads. The cited references do not disclose any of these elements.

The applicants have made a novel and nonobvious contribution to the art of 3D semiconductor memory device fabrication. The claims at issue are believed to distinguish over the cited references and to be in condition for allowance. Accordingly, such allowance is now earnestly requested.

Respectfully submitted,



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